NEW TURBO-CODE TERMINATION SCHEME FOR VARIABLE BLOCK LENGTH

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Abstract

Iterative decoding scheme (TURBO-Codes) provides the possibility to achieve results near to the Shannon limit. Here we present a new method of block decoding of TURBO-Codes where the termination of the trellis of all the used Soft-in-Soft-out decoders is possible. This leads to an improvement in the performance of the channel coding. Finally we discuss the achieved simulation results in AWGN and 60-GHz multipath channels.

1. Introduction

In many systems like MEDIAN[1] the digital data is transmitted in frames (eg. ATM cells). Mostly block codes are preferred to encode, transmit and decode the frames independently from one and other. After the introduction of the TURBO codes in [1], many results for block decoding using these codes were presented in [2], [3]. Due to the application of the 'Recursive Systematic Codes (RSC)' the difficulties in terminating the trellis of the decoders were also pointed out in [2]. With the presentation of the Turbo-Block-Codes in [4] a hurdle of terminating the trellis is overcome. By using tail bits and the polynomial division property of RSC codes illustrated in [4] we present a way to terminate both the decoders which are used in an iteration of a TURBO decoder separated by an interleaver. We also enlight the flexibility of the cell size by a fixed code polynomial. This paper is divided into 6 subsections. In the second section a brief description is given on the polynomial division property of RSC codes. After that a cell size adapted way of encoding with tail bits is explained. The section following to it demonstrates the decoding procedure. In section 5 a discussion on the achieved simulation results in AWGN and 60 GHz LOS channels using the models described in [8] is given.

2. Polynomial Division Property

Here we give a concise explanation of this property. For details please refer to [4]. All the considered polynomials *G(D)* for the recursion of the encoder have a particular polynomial *P(D)* which satisfy the equation

$$P(D) = f(D) * G(D) = 1 + D^l \qquad (1)$$

We define *P(D)* as the reset polynomial and *l* as the length of it. The division of *P(D)* by *G(D)* is aliquot. If the coderate of the encoder is restricted to '½', the selection of good polynomial combinations can be done with the equation

$$G_1(D) + G_2(D) = D * H(D), \qquad (2)$$

where the grades of $G_1(D)$ and $G_2(D)$ are equal to the memory of the encoder '*m*' and that of *H(D)* is '*m-2*'. $G_1(D)$ and $G_2(D)$ differ in the coefficients *D* and D^{m-1}. All the considered polynomials include the term '1'. This class of codes possess a large free distance and doesn't lead to catastrophic codes [5]. These codes also include some of the well know primitive polynomials. For a primitive polynomial there exists a *P(D)* with $l = 2^m - 1$.

If *G(D)* divides $1 + D^l$ without any remainder, then it also divides $1 + D^{n*l}$ where '*n*' is a natural number greater than 0. By encoding a sequence related to $1 + D^{n*l}$ through a RSC encoder starting at the zero state, the encoder will be driven back to the zero state after the end of the sequence. This property along with the linearity feature is used to terminate the trellis of the second decoder of an iteration by TURBO codes.

3. Modified TURBO-Encoder

In order to make use of the above mentioned property and the tail bits, the encoder is modified as shown in figure 1.

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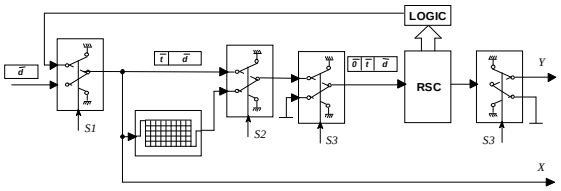

Figure 1: *Modified TURBO Encoder*

The information data '$\bar{d}$' of '*N*'-bits, where *N* represents the size of a block, is first passed through the RSC encoder and at the same time fed into an interleaver of size equal to $(N + N_t)$ with 'N_t' denoting the number of tail bits, i.e. size of '$\bar{t}$'. The interleaver should assure that each bit *d(t)* at the input should be equal to the output bit *d(t+x)*, with $x = (N + N_t + n * l)$. A logic circuit inspects the present state of the RSC encoder and generates the respective bit with which the encoder is driven to the zero state in short time. After the last information bit is passed through the coder, the 'S_1' switch selects N_t tail bits which depends on the memory of the encoder. If the sum of the data bits and the tail bits is not a multiple of the grade of reset polynomial, then 'N_0' number of zero bits '$\bar{0}$' are introduced into the data input of the RSC encoder by switching 'S_3'.

$$N_0 = i * l - (N + N_t) \geq 0 \qquad (3)$$

'*i*' is the smallest integer which satisfies the required condition. During the insertion of zero bits the clocking of the interleaver is stopped. At the same time the output of the encoder is ignored, as these bits are simply used to satisfy the polynomial division property. Once the last zero bit is passed through the encoder the reading of the interleaver data is done by selecting the 'S_2' switch. Through this modified method the number *N* is not fixed to a value which is a multiple of the length of the reset polynomial. Since the blocks are to be independent of each other, a continuous encoding is not possible.

For instance a RSC encoder with the octal representation of the polynomials {13,15} is considered. The recursion polynomial is 13. The grade *l* of the reset polynomial is 7 and requires N_t=3 tail bits. If *N* is 440 then the total size of the interleaver would be 443 with 22 rows and 21 columns where the last row consists of only three elements. The interleaver is filled with the data in rows and the reading is done column by column. This makes sure that each input bit of the interleaver is written out after (443+7**n*). If a search for an optimal interleaver is performed, then the shuffling of the order of reading is allowed only within a column. Here there is a need of 5 zero bits such that the size of input frames of the encoder is a multiple of its reset polynomial grade 7. The systematic part '*X*' now consists of the data bits and the tail bits. The redundancy part '*Y*' is punctured to obtain the required code rate.

4. Decoding of the TURBO-Codes

The construction of an iteration of the TURBO decoder is similar to that in [1]. Each iteration consists of two MAP [6] or SOVA [7] decoders in serial to realize the soft input and soft output decoding. Here we consider only the SOVA algorithm as the realization of this algorithm is less complex than that of the symbol-by-symbol MAP algorithm at a cost of small loss in the correction capacity. Both the decoders are separated by an interleaver of same size as used by the modified encoder. After the reception of a block, decoding of it is done. In decoding the modified TURBO block codes an extra information is availed. This information says that all the decoders start in zero state and terminate in the zero state. The termination of the first decoder is achieved with the tail bits. The second decoder's trellis is terminated using the polynomial division property. This art of decoding minimizes the burst errors at the end of a block which occur if the applied Viterbi algorithm selects a wrong path. This is mostly the case in block decoding with Viterbi algorithm as the observation length of the last received bits is less than thrice the memory length. Since the decoding starts in the zero state, a metric value greater than that of the other state metrics is provided to the zero state while initializing the values.

5. Simulation Results

To test the efficiency of the new modified block decoding of TURBO-Codes simulations were carried out for block length of 440 bits which is equal to an ATM cell with two extra bytes for frame informations in case of wireless transmission like in MEDIAN. Figure 2 shows the comparison of continuous and block decoding for BPSK modulation after two decoder iterations. The output of the RSC{13,

15} encoder is punctured in order to acquire code rates 1/2 and 5/7.

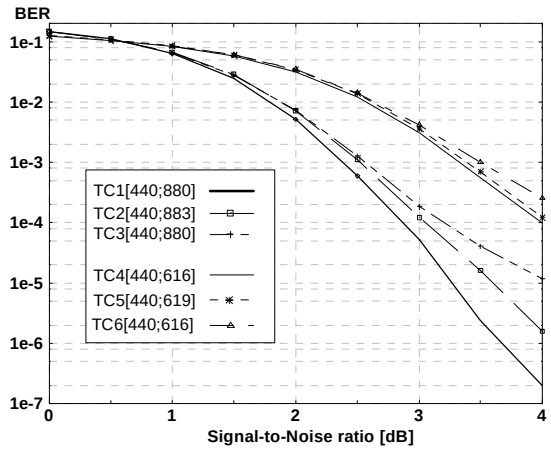

Figure 2: *Comparison of continuous and block decoding*

'TC1[440;880]' represents the continuous Viterbi decoding with SOVA, truncation path length 50 and code rate '1/2'. 'TC2[440;883]' shows the new modified decoding with the termination of trellis of all decoders where as 'TC3[440;880]' represents the art of decoding where only the second trellis of an iteration is terminated. The redundancy part of the TC2 also include the 3 tail bits to terminate the trellis of the first decoder of an iteration. Zero bits were punctured out before the transmission and introduced into the frame befor decoding making the block length to be 448. The observation length is 56 which makes it possible to flush the decoded informations after 8 loops. This assures the decoding process to be independent from block to block. Due to the flushing out process, the last informations of a block delivered by the SOVA decoder were not as relevant as the the previous informations since the observation length was less than thrice the memory length of the encoder. This leads to a degradation in the correction performance compared to the continuous decoding where each and every bit has the observation length of 50. It is also seen that the early flattening effect around bit error rate of 10^{-5} which occurs by keeping the trellis of the first decoder open is also suppressed by terminating both the decoders, but not completely removed. 'TC4[440;616]' represents the continuous Viterbi decoding for code rate '5/7'. 'TC5[440;619]' stands for the art of decoding where all the trellis of the decoders are terminated whereas 'TC6[440;616]' shows the results achieved by decoding where the trellis of 2nd decoders of itereations were terminated. The application of these codes is also tested for a wireless OFDM system with AWGN and simplified LOS model of the 60 GHz indoor radio channel presented in [8]. The synchronisation is not ideal. Figure 3 depicts the achieved results for DQPSK modulation with TURBO block codes with two iterations and Reed-Solomon Coding schemes. The code rates are nearly equal to '5/7'.

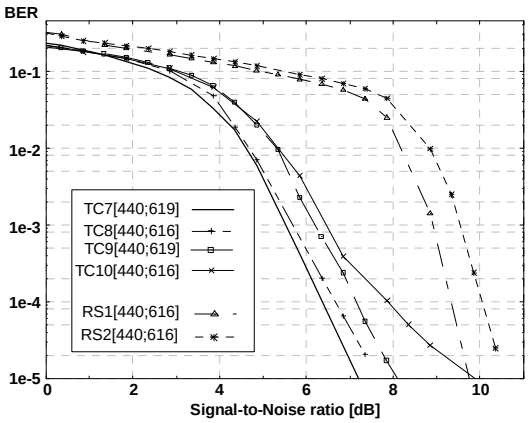

Figure 3: *Comparison of TURBO-Codes with Reed-Solomon codes for 512 subcarrier DQPSK-OFDM system in AWGN and LOS with both time and frequency error correction.*

TC7[440;619] and TC8[440;616] represents for the AWGN channel with termination of all decoders and termination of second decoder respectively. In the same way TC9[440;619] and TC10[440;616] represents for LOS channel. It is seen that for small BER the flattening effect is reduced especially for LOS channel. RS1[440;616] shows the BER for AWGN channel whereas RS2[440;616] denotes for LOS channel model. At BER of $2*10^{-5}$ the new TURBO block codes shows a gain of 2.8 dB on signal-to-noise ratio for AWGN channel compared with Reed-Solomon codes and 2.5 dB for LOS channel model.

6. Conclusions

We have shown a new art of TURBO block decoding where the termination of the SOVA decoders results in an improvement of the correction capacity of the decoder at high SNR values by suppressing the early flattening effect. This art of decoding allows to keep the block length variable for a given code polynomial. We also presented the selection of generator polynomials for the coding scheme.

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References

[1] Claude Berrou, Alain Glavieus, Punya Thitimajshima, "*Near Shannon Limit Error-Correcting Coding and Decoding (TURBO-Codes)*", International Conference on Communication (ICC), Geneva Switzerland, pp. 1064 - 1070, May 1993

[2] Patrick Robertson, "*Illuminating the Structure of Code and Decoder of Parallel Concatenated Recursive Systematic (Turbo) Codes*", Proceedings
IEEE GLOBECOM'94, San Francisco, pp. 1298 - 1303, 1994

[3] Peter Jung and Markus Nasshan, "*Performance evaluation of turbo codes for short frame transmission systems*",
Electronics Letters, Vol. 30, No. 2, pp. 111 - 113, January 1994

[4] Claude Berrou, Stéphane Evano, Gérard Battail, "*Turbo-block-codes*", Proceedings of TURBO CODING Seminar at Lund University, Sweden, pp. 1 - 8, 28-29 August 1996

[5] Farhad Hemmati and Daniel J. Costello, JR., "*Asymptotically Catastrophic Convolutional Codes*", IEEE Transactions on Information Theory, Vol. IT-26, No. 3, pp. 298 - 304, May 1980

[6] L- R. Bahl, J. Cocke, F. Jelinek, J. Raviv, "*Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate*", IEEE Transactions on Information Theory, Vol. 20, pp. 284 - 287, March 1974

[7] Joachim Hagenauer, Peter Hoeher, "*A Viterbi Algorithm with Soft Decision Outputs and its applications*", Proceedings of IEEE GLOBECOM, pp. 1680 - 1686, November 1989

[8] S. Zeisberg, B. Kull, F. Poegel, P. Pikkarainen and A. Finger, "*Channel Coding for Wireless ATM using OFDM*", Proceedings of ACTS-Mobile Telecommunications Summit, Granada, Spain, pp. 652 - 658, November 27 - 29, 1996